

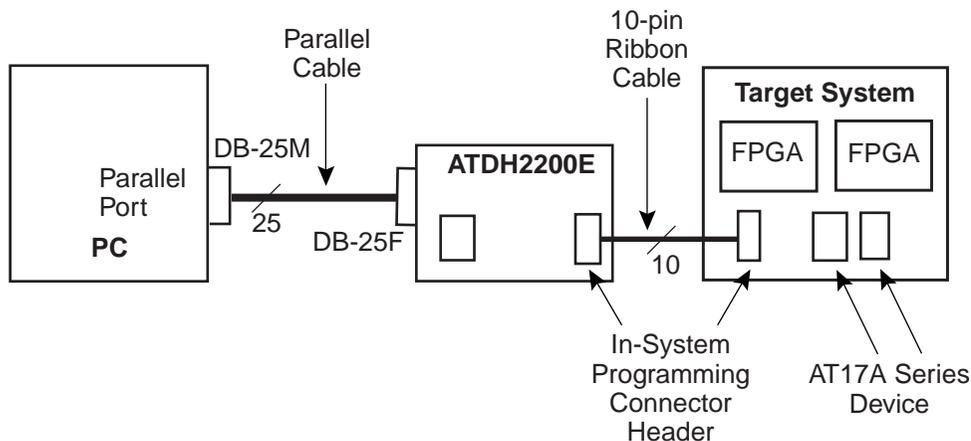


In-System Programming Circuits for AT17A Series Configurators with Altera® FPGAs

Atmel AT17A⁽¹⁾ series configurators use a simple serial-access procedure to configure one or more Altera Field Programmable Gate Arrays (FPGAs) or programmable logic devices.

This application note provides the circuits used to program Altera FPGAs with an AT17A series configurator. To perform In-System Programming (ISP), a cable is required in order to provide communication between the programmer and the configurator, see Figure 1 and Figure 2.

Figure 1. ATDH2200E In-System Programming



AT17A Series FPGA Configuration Memory

Application Note

1. AT17A=AT17F/LVXXXXA
AT17=AT17F/LVXXX



Figure 2. ATDH2225 In-System Programming

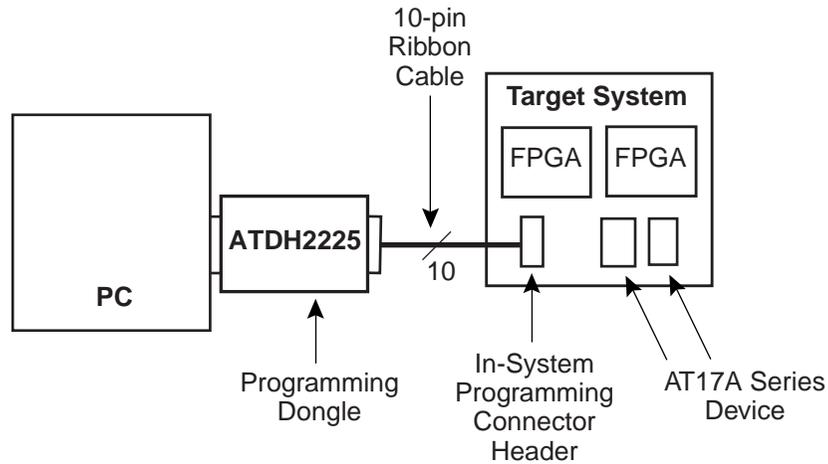
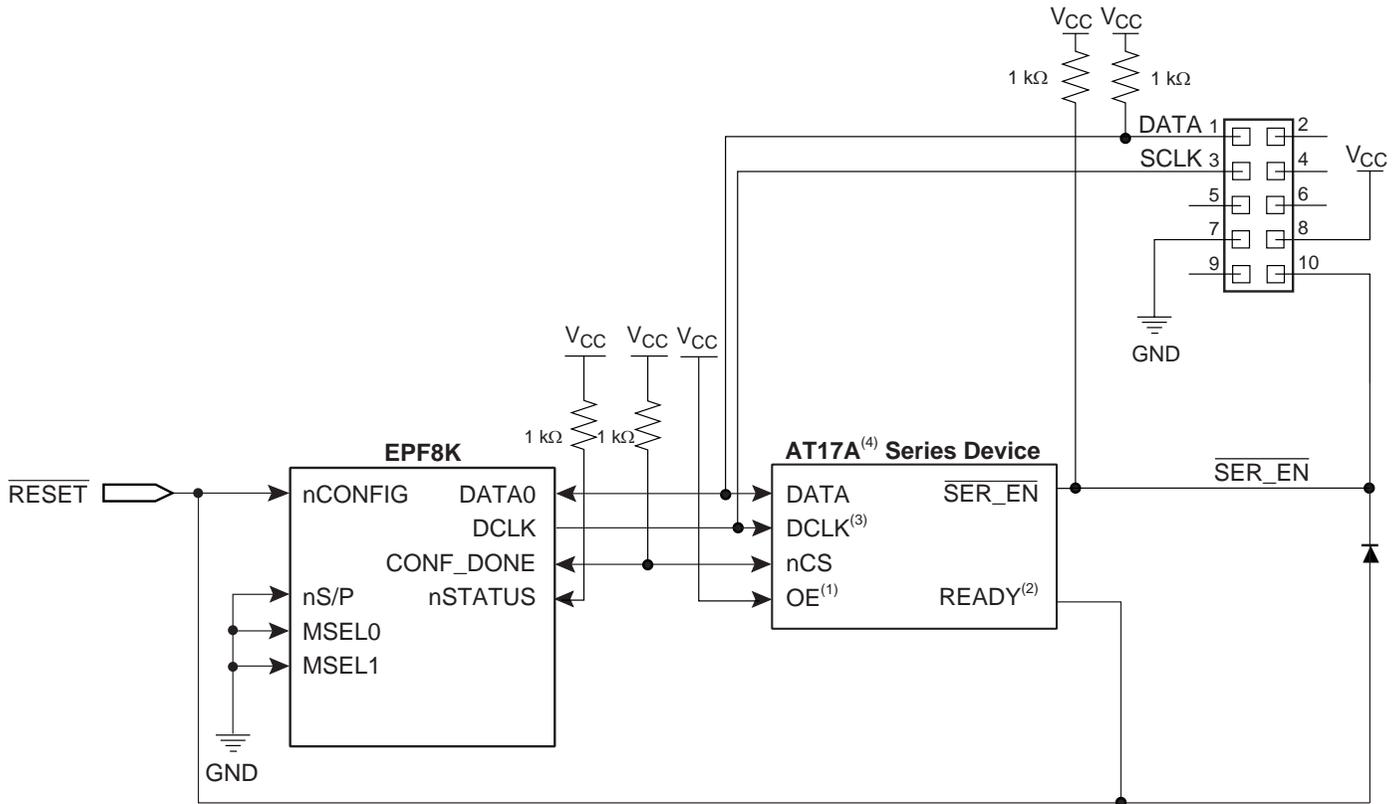


Figure 3. ISP of AT17A Series Devices for Altera EPF8K FPGA Applications



- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by an ISP programmer if a non-AT17F series device is used.
 2. Use of the READY pin is optional.
 3. For AT17LV512A/010A/002A devices, the internal oscillator of the DCLK pin must be disabled to avoid clock contention.
 4. AT17 Series devices could also be used.
 5. The A2 bit level setting in the Configurator Programming System (CPS) software must be set to High for ISP access to AT17F series devices, and Low for AT17LV series devices.



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