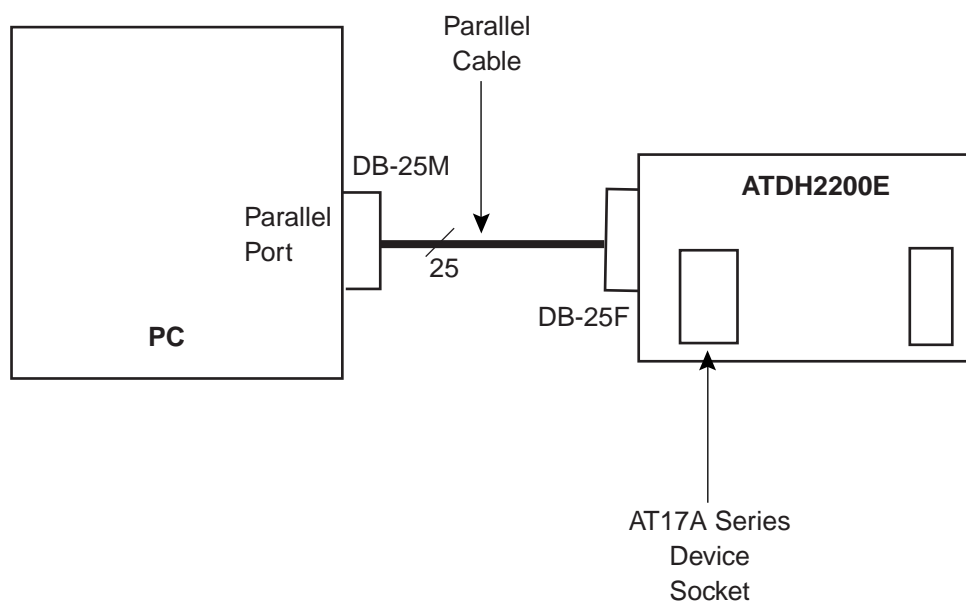


Drop-In/Stand-alone Programming Circuits for AT17A Series Configurators with Altera® FPGAs

Atmel AT17A ⁽¹⁾ series configurators use a simple serial-access procedure to configure one or more Field Programmable Gate Arrays (FPGAs) or programmable logic devices.

This application note provides the drop-in/stand-alone programming circuits for AT17A series devices Altera FPGAs. For Drop-In/Stand-alone Programming, the configurator is programmed before dropping into the circuit that will configure the FPGA, see Figure 1.

Figure 1. ATDH2200E Stand-alone Device Programming



1. AT17A=AT17LV/FXXXXA
AT17=AT17LV/FXXX



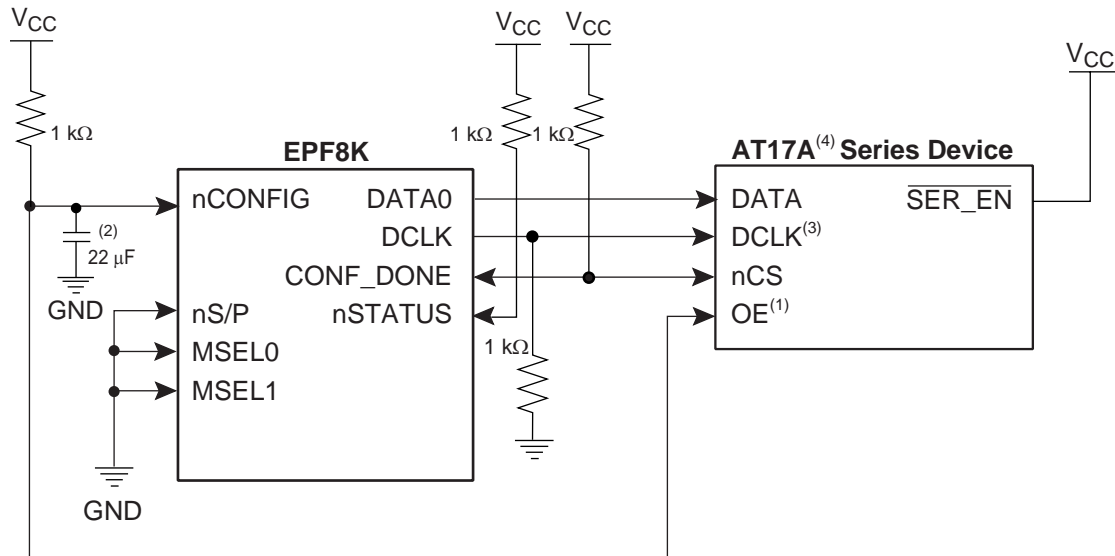
AT17A Series FPGA Configuration Memory

Application Note



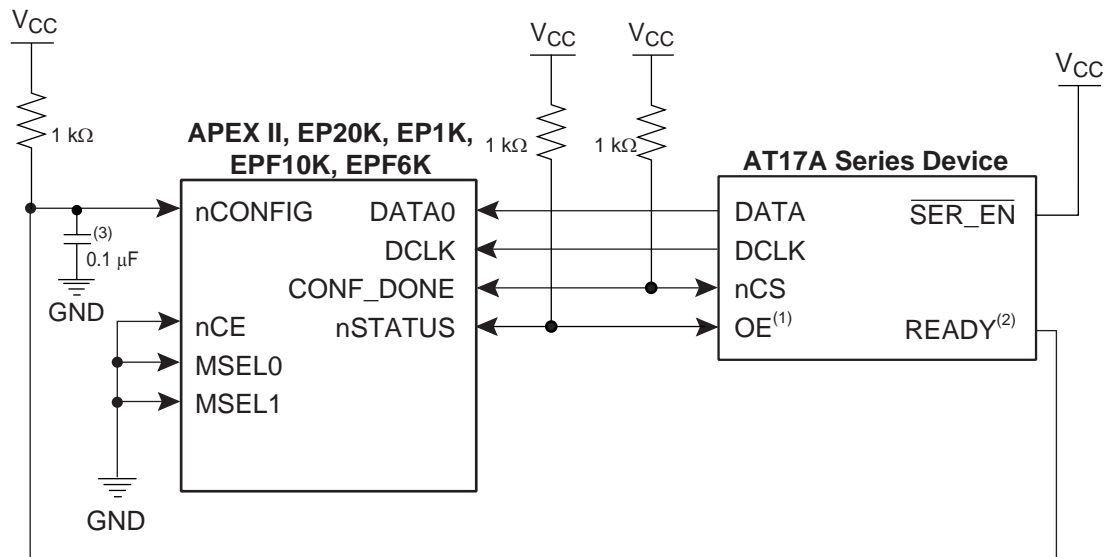
Figure 2, Figure 3 and Figure 4 show the configurator connection for different families of Altera FPGAs.

Figure 2. Drop-In Replacement of AT17A Series Devices for Altera EPF8K FPGA Applications



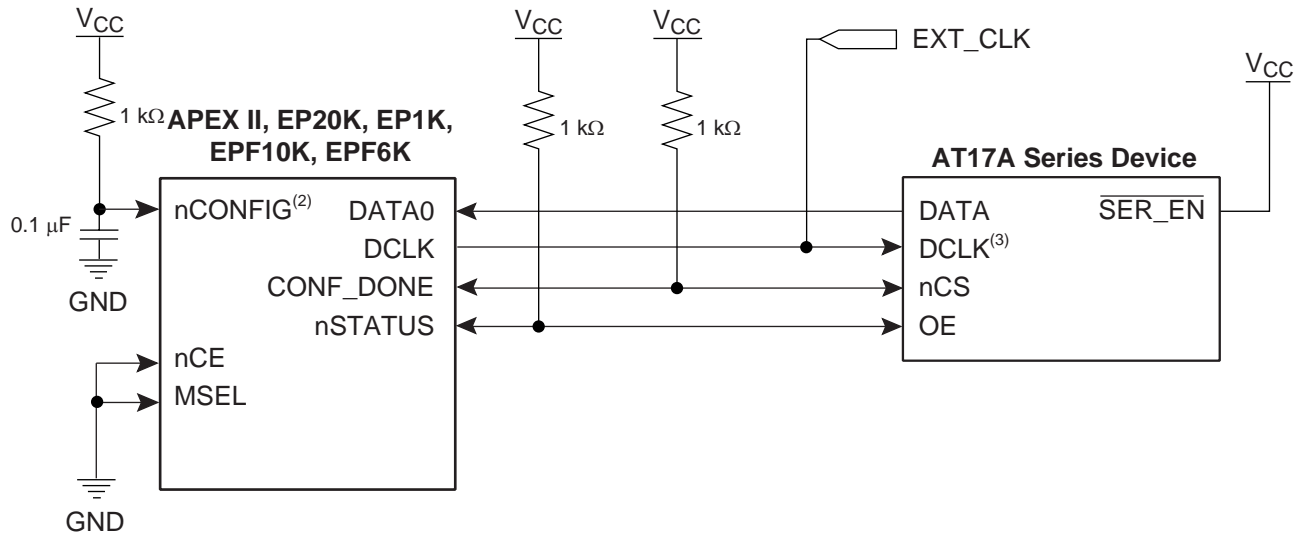
- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by a programmer.
 2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal).
 3. For AT17LV512A/010A/002A devices, the internal oscillator of the DCLK pin must be disabled to avoid clock contention.
 4. AT17 Series devices could also be used.

Figure 3. Drop-In Replacement of AT17A Series Devices for Altera FPGA Applications, Internal Oscillator Arrangement



- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by a programmer if an AT17LVXXXA series configurator is used.
 2. Use of the READY pin is optional.
 3. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal).
 4. For Altera's EDF6K FPGA, MSEL is used instead of MSEL0 and MSEL1.

Figure 4. Drop-In Replacement of AT17A Series Devices for Altera FPGA Applications



- Notes:
1. Reset polarity level of the configurator must be set to active Low ($\overline{\text{RESET/OE}}$) by a programmer if an AT17LVXXXA series configurator is used.
 2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal).
 3. For AT17LV512A/010A/002A devices, the internal oscillator of the DCLK pin must be disabled to avoid clock contention.
 4. AT17 series devices could also be used.



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